

and basic mask set to be easily adapted to provide different desired values of V_{t1} . This is a significant advantage.

[0026] FIG. 10 is a simplified plan view 94 of two ESD clamps 84, 84' of the type shown in FIG. 9 electrically cascaded or stacked in series to provide ESD clamp 86 analogous to ESD clamp 51 of FIG. 6 comprising stages 41, 41'. The same reference numbers are used in FIG. 10 as in FIG. 9 to identify similar elements, wherein the elements of lower or first ESD stage 71, 84 are the same as in FIG. 9, and those of upper or end or last ESD stage 71', 84' are identified by adding a (') to the corresponding elements. Accordingly, the discussion of FIG. 9 is incorporated herein by reference as applied to FIG. 10. Conductor 81 is adapted to be coupled to GND terminal 23 of circuit 10 of FIG. 1 and conductor 82' is adapted to be coupled to I/O terminal 22 of circuit 10 of FIG. 1.

[0027] It has been found that the arrangement illustrated in FIGS. 5-7 and 8-10 provide very useful ESD protection when applied in circuit 10 of FIG. 1, and that the values of V_{t1} can be easily adjusted to suit different circumstances, e.g., different circuit operating voltages and/or desired protection thresholds. The entries in Table I show how varying the value of resistances R in the various embodiments can be used to adjust the desired trigger voltage V_{t1} . The data of Table I was taken on ESD devices corresponding to the circuit shown in FIG. 5 and the physical implementation illustrated in FIGS. 8-9, where R_{29} and R_{39} are the values of resistors 29, 39 respectively.

TABLE I

Single Stack, Bi-directional, Resistor Triggered ESD device				
$R_{29} = R_{39} = 2 \text{ k}\Omega$	$R_{29} = R_{39} = 4 \text{ k}\Omega$	$R_{29} = R_{39} = 8 \text{ k}\Omega$	$R_{29} = R_{39} = 20 \text{ k}\Omega$	
$V_{t1} = 44.41 \text{ volts}$	$V_{t1} = 32.9 \text{ volts}$	$V_{t1} = 27.44 \text{ volts}$	$V_{t1} = 23.5 \text{ volts}$	

It will be noted that by adjusting the values of R_{29} and R_{39} , that the trigger voltage V_{t1} can be adjusted over a wide range. In general, resistor values in the range of about 0.5 k to 150 k Ohm are useful, with resistor values in the range of about 1 k to 100 k Ohms being more convenient and resistor values in the range of about 1 k to 60 k Ohms being preferred. While the data presented in Table 1 is for the case where all of the resistors in the resistor triggered ESD clamp stages were set to the same values, that is, all stages had the same value resistors (e.g., 2 k or 4 k or 8 k or 20 k Ohms) for the different tests, this is not essential and different stages may use different resistor values in order to fine tune the desired trigger voltage and/or to obtain different trigger voltages for different polarity ESD transients. This is a further advantage of using multiple resistor triggered ESD clamp stages as described herein.

[0028] FIGS. 11-12 are plots of current I in amps verses voltage V in volts for ESD clamps according to several embodiments of the invention when subjected to simulated ESD transients obtained from a charged transmission line, for example, as are routinely used for human body model (HBM) testing of ESD clamps. FIG. 11 shows I-V plot 90 for single, double and triple stack or stage ESD clamps. Trace 91 shows the I-V plot obtained for single stage ESD clamp 41 of FIG. 5 having the cross-section and plan view layout illustrated in FIGS. 8 and 9, respectively. Trace 92 shows the I-V plot obtained for double stack or stage ESD clamp 51 of FIG. 6 having the plan view layout illustrated in FIG. 10 and cross-

sectional views corresponding to two serially coupled arrangements of the cross-section shown in FIG. 8. Trace 93 shows the I-V plot obtained for triple stack or stage ESD clamp 61 of FIG. 5 having the cross-section and plan view layout corresponding to three serially coupled arrangements of ESD clamps 71 illustrated in FIGS. 8 and 9, respectively. In all three cases the resistor values R_{29} , R_{39} were set at 40 k Ohms, that is $R_{29}=R_{39}=R_{29'}=R_{39'}=R_{29''}=R_{39''}=40 \text{ k Ohms}$. V_{t1} for the single stack (trace 91) was 23.7 volts, V_{t1} for the double stack (trace 92) was 48.9 volts, and V_{t1} for the triple stack (trace 93) was 73.9 volts, illustrating how different values of trigger voltage V_{t1} (and holding voltages) may be obtained by electrically stacking ESD stages. For experimental convenience, the individual ESD stages in the two stack and three stack arrangements were substantially identical to the single stack arrangement and had the same resistance values R_{29} , R_{39} but this is not essential. It may be desirable in some situations to have resistors R_{29} , $R_{29'}$, $R_{29''}$, etc., have the same resistance values and resistors R_{39} , $R_{39'}$, $R_{39''}$, etc., have different resistance values.

[0029] FIG. 12 shows I-V plot 95 for a double stack or stage ESD clamp corresponding to the circuit of ESD clamp 51 of FIG. 6 and cross-section and plan layout shown in FIGS. 8-9 respectively, with R_{29} , $R_{39}=40 \text{ k Ohms}$ but oriented in different directions on the same wafer. The device of trace 96 was oriented at 0 or 180 degrees and the device of trace 97 was oriented at 90 or 270 degrees. Stated another way, the devices of traces 96 and 97 were oriented at right angles to each other. The device corresponding to trace 96 gave $V_{t1}=53.4 \text{ volts}$ and the device of trace 97 gave $V_{t1}=53.1 \text{ volts}$. This is an important result since it is well known in the art that ESD clamps often are orientation sensitive, that is, nominally identical ESD clamps on the same wafer or die, but with different azimuthal orientations in plan view can exhibit significantly different values of V_{t1} and I-V behavior, to the detriment of performance and manufacturing yield. The fact illustrated in FIG. 12 that the invented arrangement does not exhibit this behavior is a significant and economically important result.

[0030] The two-stack results (trace 92) of FIG. 11 with 40 k Ohm resistors gave $V_{t1}=48.9$ and the two stack results of FIG. 12 (traces 96, 97) gave $V_{t1}=53.4$ and 53.1. The difference in V_{t1} results $=(53.25-48.9)/48.9=8.8\%$ occurred because the devices of FIG. 12 were of smaller area than those of FIG. 11. While V_{t1} depends strongly on the value of resistors R_{29} , R_{39} , etc., as shown by Table I, V_{t1} is also weakly dependent on the device size, thereby providing another means for fine tuning the desired value of V_{t1} .

[0031] According to a first embodiment, there is provided an electronic device having input/output (I/O) and common terminals, comprising, a circuit core coupled between the I/O and common terminals, and one or more serially arranged resistor triggered bi-directional ESD clamp stages coupled between the I/O and common terminals. According to a further embodiment, there is only one resistor triggered bi-directional ESD clamp stage. According to a still further embodiment, each resistor triggered bi-directional ESD clamp stage comprises first and second serially coupled bipolar transistors, each bipolar transistor having an emitter, a base and a collector, and wherein the emitter of the first transistor is coupled to the common terminal and the emitter of the second transistor is coupled to the I/O terminals and the collectors of the first and second transistors are coupled together, and a first external resistor is coupled between the emitter and base of the first transistor and a second external